UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/784,722	02/23/2004	Alexandre Pierre Palus	TI-35999	9491

23494 7590 05/09/2005

TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
TRAN, ANH Q	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 05/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/784,722	PALUS, ALEXANDRE PIERRE	
	Examiner	Art Unit	
	Anh Q. Tran	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 2, 5-6, 7-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Pradhan (6,781,456).

Pradhan shows:

1. Apparatus for transferring a logic signal from a first unit (transmitter) to a second unit (LVDS receiver), the apparatus comprising:

a first conductor (INP, Fig. 3) for transferring the logic signal;

a complementary unit (inherent limitation since this is differential bus signal) for forming the complement of the logic signal;

a second conductor (INM) coupled to the complementary unit for transferring the logic signal complement; and

a verification unit (314, 306, 308, 310) coupled to the first and second conductor, the verification unit using the signals transferred by the first and second conductor to reconstitute the logic signal.

2. The apparatus as recited in claim 1 wherein the verification unit issues a preselected signal (OUT is low) when the verification unit can not reconstruct the logic signal (col. 3, lines 58-67 to col. 4, lines 32).

5. The apparatus as recited in claim 1 wherein the verification unit includes a logic EXCLUSIVE NOR gate (306, Fig. 4), the first conductor being coupled to a first input terminal (308) of the logic EXCLUSIVE NOR gate, the second conductor being coupled to a second input terminal (310) of the logic EXCLUSIVE NOR gate, the output terminal of the logic EXCLUSIVE NOR gate providing the preselected signal when an error in the transmission of the logic signal is identified.

6. The apparatus as recited in claim 1 wherein the first and second conductors are part of a bus.

The apparatus described above is applicable to the method claims 7-9.

3. Claims 1-4, and 10-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Hattori (6,593,801).

Hattori shows:

1. Apparatus for transferring a logic signal from a first unit (14, Fig. 2) to a second unit (16'), the apparatus comprising:

a first conductor (24) for transferring the logic signal;

a complementary unit (a small circle at 10) for forming the complement of the logic signal;

a second conductor (26) coupled to the complementary unit for transferring the logic signal complement; and

a verification unit (22 & 20) coupled to the first and second conductor, the verification unit using the signals transferred by the first and second conductor to reconstitute the logic signal.

2. The apparatus as recited in claim 1 wherein the verification unit issues a preselected signal (FSB is low) when the verification unit can not reconstruct the logic signal.

3. The apparatus as recited in claim 1 wherein the verification unit includes a logic AND gate (20), the first conductor coupled to a first terminal of the logic AND gate, the second conductor being coupled to an inverting terminal of the logic AND gate (FSB), the output terminal of the logic AND gate providing the logic signal in the absence of error.

4. The apparatus as recited in claim 3 wherein the output of the logic AND gate has a predetermined value (LOW) when an error is detected.

10. The automotive system for exchanging logic signals in an automotive unit, the system comprising:

a central processing unit (control logic consider as a processing unit, col. 1, line 37);

at least one peripheral unit (16'); and a bus coupling the central processing unit and the peripheral unit, the bus including a first (24, Fig. 2) and a second conductor (26);

wherein a signal transmitting unit includes an a logic signal inverting device (a small circle at 10) coupled to the second conductor, the transmitting unit applying a logic signal to the first conductor and to an input terminal of the logic signal inverting device;

wherein a signal receiving unit includes combining unit (22 & 20), the combining unit combining the signals on the first and second conductor to provide the logic signal when an error has not occurred to the signals transmitted by the first and second conductors (col. 1, lines 55-60).

11. The system as recited in claim 10 wherein the unit for combining includes a component for generating a preselected signal (LOW) when an error has occurred in the transmission of a signal on one of the first or second conductors.

12. The system as recited in claim 10 wherein the combining unit includes a logic AND gate (20), the first conductor being coupled a first input terminal of logic AND gate, the second conductor being coupled to a second and inverting input terminal (FSB) of the logic AND gate.

13. The system as recited in claim 11 wherein the component a logic EXCLUSIVE NOR gate (40, Fig. 5A), the first conductor (Z) being coupled to a first input terminal of the logic EXCLUSIVE NOR gate, the second conductor (Z) being coupled to a second input terminal of the logic EXCLUSIVE NOR gate.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh Q. Tran whose telephone number is 571-272-1813. The examiner can normally be reached on M-TH (7:00-5:30) Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANH Q. TRAN
PRIMARY EXAMINER

5/5/05